## Biography

Te-Kuang Chiang, Professor and Doctoral Supervisor of the Advanced Device Simulation Laboratory of National Kaohsiung University, LSI IC design Engineer of the United States, Senior Member of IEEE, Senior Member of the Chinese Engineering Education Association (IEET), Member of the Special Case Examination Committee of the Ministry of Science and Technology of Taiwan, and the Patent Examination Committee of Taiwan， IEEE Tainan EDS Vice President of the Chapter. Chiang Te-Kuang served as a reviewer for IEEE Trans on Electron Device， IEEE Electronic device letter， IEEE Material and device reliability， Solid-state Electronics， IEEE Trans on Nanotechnology， Journal of Microelectronics， Microelectronics Reliability， International Journal of Numerical Modeling ， Semiconductor Science and Technology， Applied Physics letter， Journal of Computational Electronics， Journal of Japanese Applied Physics， IEEE Express， Micro and nanostructure etc. and other international journals and magazines. Te-Kuang Chiang specializes in the characteristic analysis, simulation and modeling of integrated circuit devices. Focus on the subthreshold behavior modeling of multiple gates（MG）field-effect transistor (FET) containing a double-gate（DG）MOSFET， Surround-gate MOSFET （SRG） MOSFET， FinFET MOSFET， Quadruple-gate (QG) MOSFET, Pi-gate （Pi-G） MOSFET. This theory was further applied to low-power and low-voltage integrated circuits. There are also many research results Published in IEEE Trans on Electron Device （TED）、IEEE Electronic Devices Letter （EDL）、IEEE Trans on Material and Device Reliability （TDMR）, Solid Electronics（SSE）、IEEE Trans on Nanotechnology （TNANO）、Semiconductor Science and Technology（SST）、micro and nanostructure、Nanotechnology and other well-known SCI international journals。 Currently, the primary research focuses on the 2nm complementary FET (CFET) composed of gate-stacked nanosheet, including nanosheet Ballistic model and modeling, simulation, and design of low-power circuits.